REMARKS

Claims 1-9 and 19-24 are pending in the present application. Claims 10-18 are cancelled above as being drawn to non-elected claims. Claims 1, 2, 6, 9, and 24 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

Applicant notes with appreciation that the Office Action indicates at paragraph 6 that claims 3-5, 7, 21-22 and 24 would be allowable if rewritten in independent form. Applicant wishes to defer submission of these claims, pending consideration of the present Amendment.

Claims 1, 6, 9, 19-20 and 23 stand rejected as being anticipated by Suemura *et al.* (U.S. 5,887,039 - hereinafter "Suemura"). Claim 8 stands rejected as being unpatentable over Suemura (U.S. 5,887,039). Claim 2 stands rejected as being unpatentable over Suemura in view of Sakamoto, *et al.* (U.S. 6,557,110 - hereinafter "Sakamoto"). Reconsideration of the rejections and allowance of the claims are respectfully requested.

It is respectfully submitted that Suemura fails to teach or suggest the present invention as claimed in amended claim 1. In particular, Suemura fails to teach a "transmitter" that "includes a transmitter phase locked loop that, in response to a clock signal, generates a first plurality of non-overlapping clock signals, the transmitter for skew-compensating signals received from the video controller, for compressing the skew-compensated signals in response to the first plurality of non-overlapping clock signals, and for converting the compressed signals to a driving current" (emphasis added), as claimed in amended claim 1. This feature is described at least in FIG. 2 of the present specification, which shows the "transmitter PLL" 270 generating a plurality of 'n' non-overlapping clock signals CKP that are applied to the data serialization unit 240. The data serialization unit 240 in turn compresses applied parallel data output from the "scrambler" 220 in response to the non-overlapped clock signals CKP generated by the PLL 270 (see, for example, specification, page 10, lines 3-17). Suemura makes no mention of generating such a "first plurality of non-overlapping clock signals" as claimed in amended claim 1. Nor does

Suemura teach or suggest compressing the "skew-compensated signals "in response to the first plurality of non-overlapping clock signals" as claimed in amended claim 1.

In addition, Suemura fails to teach or suggest "a receiver that includes a receiver phase locked loop that generates a second plurality of non-overlapping clock signals in response to a received clock included in the received optical signal for converting the current signal into a voltage signal, for decompressing the voltage signal in response to the second plurality of non-overlapping clock signals ..." (emphasis added), as claimed in amended claim 1. This feature is described at least in FIG. 8 of the present specification, which shows the "receiver PLL" 88 generating a plurality of 'n'non-overlapping clock signals CKP that are applied to the data restoration and skew compensation unit 82. This unit 82 in turn decompresses applied serial data received from the "optical receiver" 80 in response to the non-overlapped clock signals CKP generated by the PLL 88 (see, for example, specification, page 20, lines 14-23, and page 37, lines 4-6). Suemura makes no mention of generating such a "second plurality of non-overlapping clock signals" as claimed in amended claim 1. Nor does Suemura teach or suggest "decompressing the voltage signal in response to the second plurality of non-overlapping clock signals" as claimed in amended claim 1.

In view of the above, it is respectfully submitted that Suemura fails to anticipate amended independent claim 1. Removal of the rejection and allowance of claim 1 are respectfully requested.

With regard to the rejection of independent claim 19, it is submitted that Suemura fails to teach or suggest, a "data restoration and skew compensation unit in a receiver" that includes a "phase locked loop for generating first through n-th non-overlapped clock signals, each having a predetermined offset to prevent mutual overlapping" (emphasis added), as claimed in claim 19. It is further submitted that Suemura fails to teach or suggest the receiver "restoring data in which n-bit synchronous signals (where n is a positive integer greater than or equal to 1) and n-bit information data are multiplexed and transmitted in series via a transmission channel, in response

to the first through n-th non-overlapped clock signals,"as claimed in claim 19. Suemura further fails to teach or suggest "latching received serial data in units of n+N-1 (where N is a positive integer greater than or equal to 3) bits in parallel in response to the first through n-th non-overlapped clock signals" (emphasis added), as claimed in claim 19. Suemura further fails to teach or suggest "latching in parallel the N state data in response to an X-th ($1 \leq X \leq n$) non-overlapped clock signal having the greatest timing margin among the first through n-th non-overlapped clock signals", as claimed in claim 19. There is no teaching or suggestion in Suemura that non-overlapped clock signals are used in this manner in the receiver, nor is there a teaching or suggestion that a determination of the non-overlapped clock signal "having the greatest timing margin" is made in Suemura. Further, there is no teaching or suggestion in Suemura of a "synchronizer" that outputs "state data from which the synchronous signal is detected ... in response to ... the X-th non-overlapped clock signal". As described above, a determination of the "X-th non-overlapping clock signal" that has the "greatest timing margin" is not made in Suemura.

In view of the above, it is respectfully submitted that Suemura fails to anticipate amended independent claim 19. Removal of the rejection and allowance of claim 19 are respectfully requested.

With regard to the rejection of independent claim 23, it is submitted that Suemura fails to teach or suggest "(a) generating first through n-th non-overlapped clock signals, each having a predetermined offset to prevent mutual overlapping, on the basis of the clock signal"; "(b) latching received serial data in units of n+N-1 (where N is a positive integer greater than or equal to 3) bits in parallel in response to the first through n-th non-overlapped clock signals"; or "(d) latching in parallel the N state data in synchronization with a X-th ($1 \leq X \leq n$) non-overlapped clock signal having the greatest timing margin among the first through n-th non-overlapped clock signals". As explained above, Suemura fails to teach or suggest generation of such "non-overlapped clock signals", and further fails to teach or suggest determining which one of the non-overlapped clock signals has the "greatest timing margin".

In view of the above, it is respectfully submitted that Suemura fails to anticipate amended independent claim 23. Removal of the rejection and allowance of claim 23 are respectfully requested.

With regard to the various dependent claims, it follows that these claims should inherit the allowability of the independent claims from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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